REMARKS

The claims are claims 13 and 29.

Claim 13 is amended. Claims 1 4, 5 and 11 are newly canceled. New claims 24 to 29 are added. Claim 13 is amended to recite the mid-position carry input it to a predetermined bit of the adder/subtractor. Claim 13 is further amended to change a recitation of "arithmetic circuit" to "adder/subtractor circuit" as previously amended. New claim 24 recites a single pair of multipliers as illustrated in Figures 4, 5 and 6 of this application. New claims 25 and 26 recite the alternatives of addition and subtraction in the adder/subtractor. New claim 27 recites additional shifters disclosed in the application at page 25, line 27 to page 26, line 5 and illustrated in Figure 6. New claim 28 recites use of the redundant sign/magnitude format and a converter as disclosed in the application at page 21, lines 23 to 24, page 22, lines 10 to 12, page 23, lines 11 to 23, page 25, lines 27 and 28, page 26, lines 21 and 22, and page 27, liens 6 to 11.

Claim 13 was rejected under 35 U.S.C. 101 as reciting non-statutory subject matter. The OFFICE ACTION states that this claim "merely disclose a step of performing a dot product by combining products of input operands without disclosing a practical application or its tangible result."

Claim 13 is statutory subject matter. Claim 13 is not a method claim as implied by the language of the OFFICE ACTION. Claim 13 is an apparatus claim reciting a particular combination of tangible parts. In particular, claim 13 recites the tangible parts of storage circuitry, a multiply circuit, an adder/subtractor circuit and a shifter. By reciting tangible, physical parts claim 13 does not merely disclose "steps of performing...without disclosing a practical application or its

tangible result." Accordingly, claim 13 is statutory subject matter.

Claim 13 was rejected under 35 U.S.C. 103(a) as made obvious by the combination of Saishi et al U.S. Patent No. 6,167,419 and Pitsianis et al U.S. Patent Application Publication No. 2003/00088601. The OFFICE ACTION states that Saishi et al discloses rounding the combined product to form an intermediate result via an arithmetic circuit having a first input receiving first product, and a carry input to a mid-position receiving rounding value to form the intermediate result at elements 803, 806, and 807 in Figure 8 and column 8, lines 11 to 63.

Claim 13 recites subject matter not made obvious by the combination of Saishi et al and Pitsianis et al. Claim 13 similarly recites "an adder/subtractor circuit having a plurality of inputs each connected to receive a corresponding one of the plurality of products from the plurality of multipliers and a mid-position carry input to a predetermined bit for mid-position rounding responsive to the rounding dot product instruction." The innovation of the application is combining operations normally requiring two hardware circuits into a single hardware circuit. The two combined operations are the sum/difference of the two products and rounding the result. The Applicants respectfully submit that the recited adder/subtractor circuit corresponds to: adder/subtractors 420, 520 and 620 disclosed in this application; addition means 109, addition means 209, first subproduct addition means 306/second subproduct addition means 308, first subproduct addition means 406/second subproduct addition means 408, first subproduct addition means 506/second subproduct addition means 508 disclosed in Saishi et al; and subtractor 623, adder 625, adder 723, subtractor 725, adder block 1723, adder block 1725, adder block 1823 and adder block 1825 of Pitsianis et al. Neither Saishi et al nor Pitsianis et al teach

combining two products and rounding in a single adder/subtractor circuit as recited in claim 13. Firstly, Saishi et al teaches only one product. Saishi et al teaches rounding the multiplication result 104 in addition means 109 and rounding the multiplication result 204 in addition means 209. Figures 3 to 5 of Saishi et al illustrate combining the partial product sums of a single product computation with rounding in first subproduct addition means 306/406/506. Thus Saishi et al fails to teach the claimed combination of two products and rounding recited in claims 1 and 13. Pitsianis et al teaches production of two products but does not teach a single adder/subtractor circuit combining two products and rounding. Figure 6 of Pitsianis et al teaches combining products in subtractor 623 and adder 625, and rounding the selection and rounder circuit 627. Figure 7 of Pitsianis et al teaches combining products in adder 723 and subtractor 725, and rounding in selection and rounder circuit 727. Figure 17 of Pitsianis et al teaches combining products in adder block 1723 and adder block 1725, and rounding in selection and rounder circuit 1727. Figure 18 of Pitsianis et al teaches combining products in adder block 1823 and adder block 1825, and rounding in selection and rounder circuit 1827. The Applicants respectfully submit that both Saishi et al and Pitsianis et al teach the adder/subtractor circuit recited in claim 13 without teaching the particularly recited combination of two products and rounding. Accordingly, claim 13 is not made obvious by the combination of Saishi et al and Pitsianis et al.

Claims 13 recites further subject matter not made obvious by the combination of Saishi et al and Pitsianis et al. Claim 13 recites "a mid-position carry input to a predetermined bit for mid-position rounding responsive to the rounding dot product instruction." Saishi et al fail to teach this use of a mid-position carry input to a predetermined bit for the recited

rounding. Saishi et al states at column 8, lines 27 to 35 (within the portion cited in the OFFICE ACTION):

> "When the range indicated by the bit range 804 of the multiplication result 803 is desired to be cut out, and when it is assumed that the predetermined rounding position 811 is basically located at the mth bit from the least significant bit in consideration of the fact that a shift count required for a shift operation for cutting out is indicated by a right shift 809 of kbits, a signal having '1' at the (m+k)th bit is generated as the rounding signal. In other words, the rounding position is shifted to the left by k bits."

This clearly teaches that the rounding position is selected by the rounding generator generating a rounding signal shifted to correspond to the later shift of the rounded product. One skilled in the art would understand the recited "shifted to the left by k bits" to be a multibit signal having 0's shifted into the k least significant bits to place a single 1 bit in the desired rounding position. Figures 1 to 5 of Saishi et al show this rounding signal applied to a normal data input of an addition means. Saishi et al never states that the rounding signal is input to "a mid-position carry input to a predetermined bit" as recited in claim 13. The FINAL REJECTION fails to cite any portion of Saishi et al as making obvious the recited mid-position carry input to a predetermined bit. One skilled in the art would understand Saishi et al to teach supply of a multi-bit rounding signal to an ordinary multi-bit data input of the adder. The left shifted 1 generated by the rounding signal generator is thus supplied to a data input and not to the carry input of a predetermined bit recited in claim 13. Thus Saishi et al teaches achieving the same result of this invention using a different method step or different apparatus. While the OFFICE ACTION states that this is disclosed in Saishi et al, in fact neither

addition means 109, addition means 209, first subproduct addition means 306, first subproduct addition means 406, nor first subproduct addition means 506 illustrate the "mid-position carry input to a predetermined bit" recited in claim 13. The description of these parts in Saishi et al indicates that the rounding signal is supplied to a data input of the corresponding addition means. Saishi et al states at column 6, lines 11 to 14:

> "The multiplication result 104 and the rounding signal 106 are input to the addition means 109, and the addition means 109 outputs the multiplication result 110 obtained after rounding."

Saishi et al states at column 10, lines 50 to 53:

> "The subproducts 305 and the rounding signal 315 are added by the first subproduct addition means 306."

This disclosure with the teaching of Saishi et al that the rounding signal is "shifted to the left by k bits" makes clear that the rounding signal is supplied to each bit of a multi-bit input of addition means 109, addition means 209, first subproduct addition means 306, first subproduct addition means 406 and first subproduct addition means 506 rather than the "mid-position carry input to a predetermined bit" recited in claim 13. The OFFICE ACTION does not allege that Pitsianis et al makes obvious this subject matter. Accordingly, claim 13 is not made obvious by the combination of Saishi et al and Pitsianis et al.

The RESPONSE TO ARGUMENTS of the OFFICE ACTION cites first addition means 406 of Figure 4 of Saishi et al as teaching the recited adder/subtractor with the mid-position carry input. The Applicant submits that first addition means 406 of Saishi et al fails to add two products as required in claim 13. Saishi et al states at column 11, lines 27 to 31:

> "numeral 406 designates a first subproduct addition means as a component of the multiplication means 403, numeral 407 designates an intermediate register for temporarily storing an intermediate result obtained in the first subproduct addition means 406"

Thus Saishi et al clearly teaches that element 406 is part of a multiplier. Thus this element cannot make obvious the recited adder/subtractor of claim 13. Accordingly, this disclosure of Saishi et al fails to teach a single adder/subtractor adding plural products and performing the rounding recited in claim 13.

The OFFICE ACTION states at page 5, lines 9 to 11:

> "In the current claim language, it does not define or require that a single integrated adder is used to combine two products and round the result,"

The Applicant respectfully submits this statement can only be made by ignoring the language of claim 13 which clearly does recite such a limitation.

New claims 25 to 29 are not made obvious by the combination of Saishi et al and Pitsianis et al. New claim 25 recites "a mid-position carry input to a predetermined bit" in the same manner as claim 13 and is likewise allowable. New claim 25 recites "a '1' input at said mid-position carry input of said predetermined bit" in manner differing from Saishi et al and Pitsianis et al. New claim 27 recites first and second ganged Q shifters illustrated in Figure 6. These shifters are not taught in the references. New claim 28 recites using the redundant sign/magnitude format and conversion to a normal coded format in a manner not taught in the references.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore

early entry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

Texas Instruments Incorporated
P.O. Box 655474 M/S 3999
Dallas, Texas 75265
(972) 917-5290
Fax: (972) 917-4418

Respectfully submitted,

/Robert D. Marshall, Jr./
Robert D. Marshall, Jr.
Reg. No. 28,527